DERWENT-ACC-NO: 2002-087372
DERWENT-WEEK: 200212

TITLE: MOS transistor and DRAM device fabrication

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PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 1999KR-0036362 (August 30, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2001019774 A	March 15, 2001	N/A	001	H01L 027/108

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001019774A	N/A		
1999KR-0036362		August 30, 1999	

INT-CL_(IPC): H01L027/108

ABSTRACTED-PUB-NO: KR2001019774A
BASIC-ABSTRACT: NOVELTY - A method for fabricating a MOS transistor having a gate line width less than 0.1 micrometer and a method for fabricating a DRAM device are provided to prevent an undesirable bridge or cut of a photoresist pattern and to improve uniformity of a line width of the photoresist pattern.

DETAILED DESCRIPTION - In the fabricating method for the MOS transistor, an

oxide pattern is formed on an active region of a semiconductor substrate (200).
A gate oxide layer is then formed on the oxide pattern and the substrate (200),
and a conductive layer is formed on the gate oxide layer. The conductive layer
is then anisotropically etched to form a conductive sidewall spacer on a
sidewall of the oxide pattern. The oxide pattern is then removed, and impurity
ions are implanted into the active region to form source/drain (216a,216b).
The fabricating method for the MOS transistor can be preferably applied to the
fabrication of the DRAM device.

CHOSEN-DRAWING: Dwg.1/10

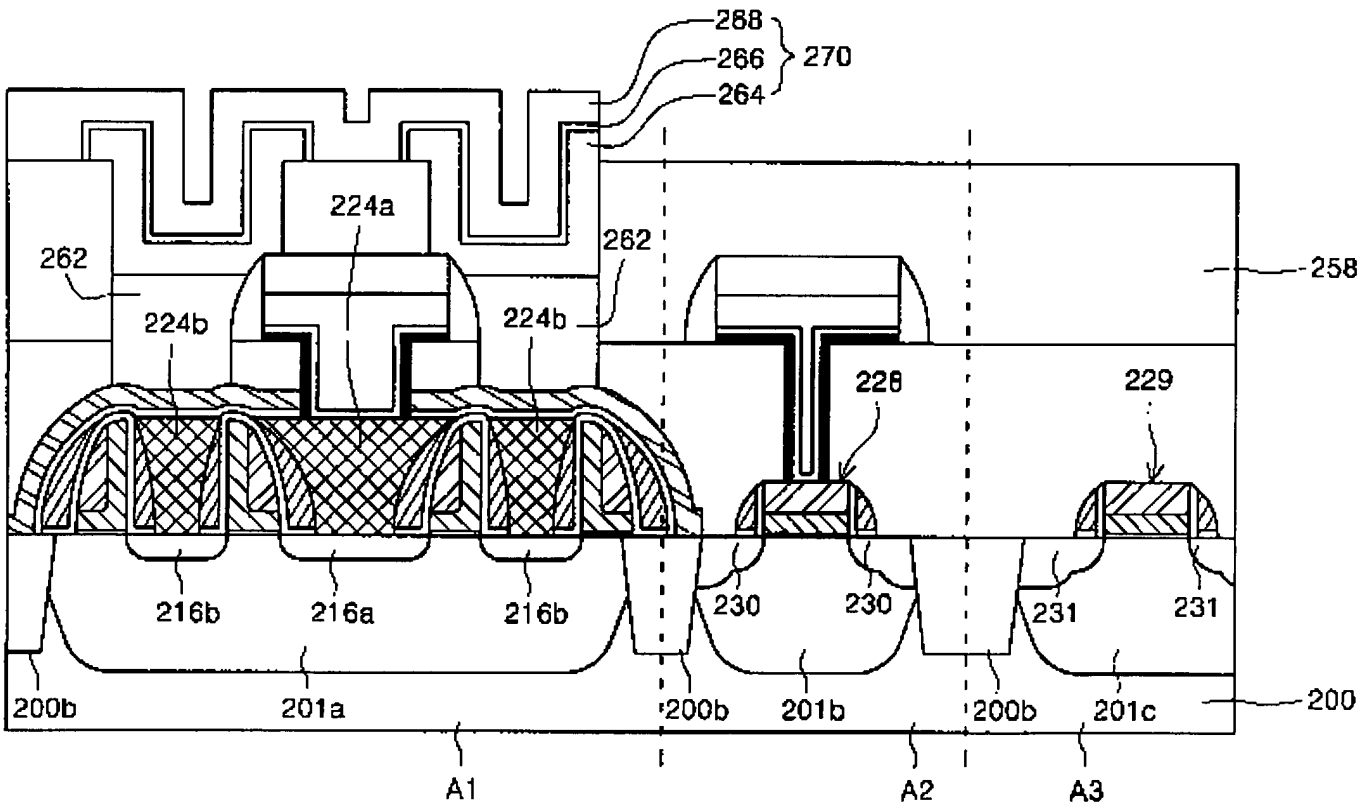
TITLE-TERMS:
MOS TRANSISTOR DRAM DEVICE FABRICATE

DERWENT-CLASS: L03 U11 U13

CPI-CODES: L03-G04A; L04-E01B;

EPI-CODES: U11-C05D4; U11-C05F1; U11-C18A3;
U11-C18B5; U13-C04B1A;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2002-026771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